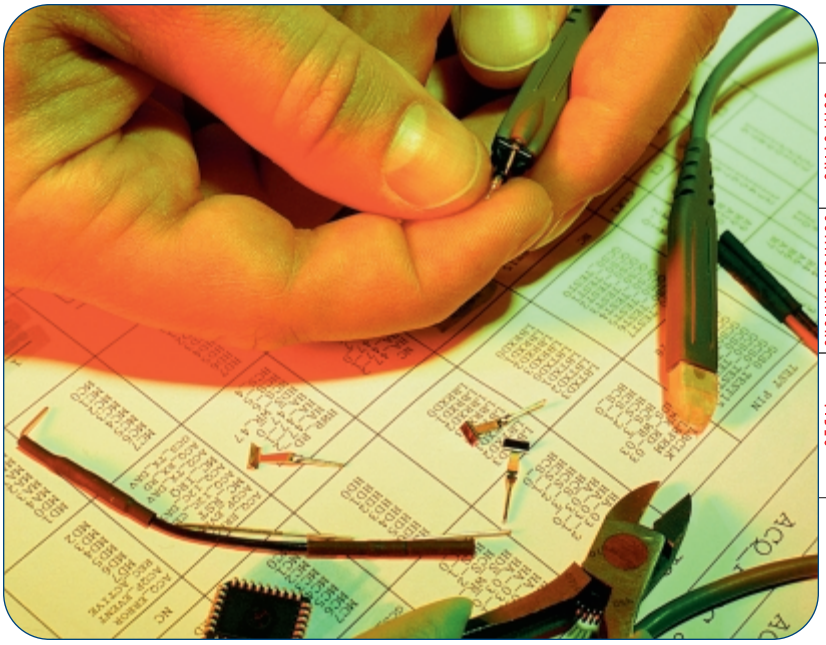
TekConnect™ Probes: Signal Fidelity Issues and Modeling



The TekConnect interface between high performance Tektronix probes and oscilloscopes provides a new probe connection standard with sufficient bandwidth to address the needs of signal integrity measurements. Understanding high performance probe measurement issues and modeling techniques is important in improving signal fidelity.

High Performance Design and Measurement

The seemingly endless desire for performance in both the digital design and communication markets has led to continuing increases in clock rate and circuit density. These performance increases have resulted in significant changes in design practices as engineers have been forced to pay increasing attention to signal integrity issues in order to produce reliable designs. Although signal integrity guidelines and even simulation tools are increasingly being used to aid the designer in the layout of high performance circuit boards, the wise designer will want to verify the performance of his design with electronic measurement tools. Just as today's high performance designs require consideration of signal integrity issues in the design process, similar consideration must be given to signal fidelity issues in the measurement process. And just as design simulation for signal integrity is becoming an increasingly important part of the circuit layout process, modeling of probe loading effects and probe measurement response are becoming a more critical part of the measurement process.

Signal Integrity Overview

In the early days of digital logic design, many designs did not require careful layout practices in order to perform reliably. The relatively slow rise times of the logic gates at that time allowed the use of manufacturing techniques such as IC sockets and wire wrap interconnections that cannot be tolerated in today's high performance designs. Although there is no exact definition of a "high performance design," in this paper a high performance design is considered one where the signal interconnect design is a critical part of the final design performance. In general, a high performance design is one in which transmission line effects must be taken into consideration during the physical layout of the design. The noise problems that arise because of the physical layout of a high performance design are commonly referred to as signal integrity problems. Signal integrity problems arise because of the finite propagation speed of signals. When the propagation delay of a signal between its interconnection points becomes comparable to the signal rise time, signal integrity issues must be taken into consideration. The signal integrity issues that will be reviewed briefly in this paper are:

- Reflection noise
- Crosstalk noise
- Power/Ground switching noise

Since dealing with signal integrity issues has become a critical part of high performance designs, circuit board design tools have become available to assist the designer with the layout process. The most recent of these layout tools use simulation techniques to analyze and, in some cases, direct the layout process. The signal integrity simulation tools extract from the layout topology the parameters that contribute to reflection, crosstalk, and power/ground switching noise.

Although the signal integrity simulation tools available today can help the designer deal with potential signal integrity noise problems, the quality of the simulation results is dependent on a number of input parameters and should eventually be verified with physical measurements. For example, the transmission line analysis of interconnects on the circuit board is dependent on the spacing between traces and the closest plane layer, as well as the dielectric constant of the circuit board material. Variations in the physical processing of the circuit board and the materials used in its construction, however, can affect both trace spacing and the board dielectric constant. The rise time of output drivers in circuit board components is also quite dependent on integrated circuit process variations and, to some degree, environmental factors.

Since the rise time of signals has a direct effect on signal integrity noise problems, at least some verification of signal integrity simulations should be done to give confidence that the simulations match reality to avoid problems from marginal performance.

The same interconnect parasitics that contribute to signal integrity noise problems in high performance designs can also contribute to measurement inaccuracies. Depending on the rise time of the signal to be measured and the physical topology of the signal net, a probe may need to be considered a parasitic component when it is attached to the signal measurement node. It is also not an uncommon problem to find that poor high frequency probing techniques result in measurement abnormalities that are incorrectly attributed to design problems. The use of measurement equipment with inadequate response speed and accuracy can also lead to errors in interpreting signal performance. The accuracy of probe measurements will be referred to in this paper as signal fidelity. Understanding the issues that can contribute to poor signal fidelity is a necessity in high performance designs. Signal fidelity issues include not only the basic performance of the measurement system, but also the loading effects of probing a circuit. The signal fidelity issues in high performance probe measurements that will be reviewed in this paper are:

- Probe bandwidth/rise time
- Probe dynamic range
- Probe loading
- Probe grounding
- Probe resonant effects

Maximizing signal fidelity requires both the careful choice of measurement equipment and the careful application of that equipment in the acquisition of signals. Only when signal fidelity issues are understood and accounted for can a designer trust that his measurements give an accurate representation of the signals present in a high performance design.

An ideal probe would allow measurements to be made with no effect on the circuit being probed and with complete accuracy in representing the signal being measured. Since ideal probes are only found in an ideal world, real world signal fidelity issues must be understood and careful measurement techniques applied so that the circuit response rather than the probe response is measured. Modeling the effect of probe parasitics in loading a measurement node is not new (see References, page 27), but the modeling task becomes more complex with high

performance measurements. Probe loading models will beintroduced in this paper that are more accurate than the simple RLC models that have been presented in the past. The effect of probe bandwidth and rise time on the response of measured signals has also been presented in the past, but generally only with a guideline to always use a probe with three to five times the bandwidth of the signal to be measured. Since today's high performance designs make it difficult, if not impossible, to find a probe with high enough bandwidth to meet that guideline, the probe models introduced in this paper should allow the designer to simulate the effect of probe performance and loading on the signal to be measured.

The Signal Integrity Challenge— High Performance Design Issues

Interconnects have become a critical design factor in high performance digital designs. An ideal interconnect would have no RLC parasitics, zero propagation delay, or interaction with other interconnects. Because the laws of physics govern interconnects, an interconnect with these ideal parameters does not exist. Depending on the length of the interconnect and the speed of the signal propagating on the interconnect, however, some of the non-ideal behavior can be ignored. In the case of very slow signals, where the signal rise time is much slower than the signal propagation time on the interconnect, the interconnect parasitics can be ignored and the interconnect can be considered to be ideal. For somewhat faster signals propagating on short interconnects, where signal propagation delay on the interconnect must be considered, a lumped circuit model can be used where only the source resistance and a lumped capacitance representing the parasitic capacitance on the net must be considered. For even faster signals, or where a more detailed simulation is needed, the lumped circuit model might need to be additionally refined to include the effect of parasitic inductance. For the highest performance digital designs, the speed of the signals ultimately requires that a more complex distributed circuit model be used, even for relatively short interconnects.

Distributed circuit analysis adds the dimension of distance to the dimensions of voltage and time used in lumped circuit analysis. An interconnect must be considered a transmission line if a time varying voltage also varies significantly with distance along the length of the interconnect. A signal propagates on a transmission line with a propagation velocity that depends on the physical properties of the material around the transmission line, and is typically only somewhat slower than the speed of light. For a microstrip transmission line on FR-4 circuit board material, the propagation velocity is about 150 ps/inch, which is about half the speed of light. For a signal rise time of 500 ps, the length of transmission line over which the rise time variation of the signal can be observed is about three inches (length = signal rise time/propagation velocity). A conservative guideline that can be applied is that an interconnect can be expected to show transmission line effects for interconnects longer than 1/6 the length over which the signal variation propagates (0.5 inch for the microstrip transmission line example).

If transmission line effects are not considered in the interconnection of fast rise time signals or long, heavily loaded signal paths, then timing or noise problems can lead to design failure. Because interconnection

delay is now a significant, if not the dominant, time delay in high performance digital designs, trace routing distances must be carefully monitored during circuit board layout. This is particularly important for clock signals in synchronous designs, where clock routing paths must be carefully matched so as not to introduce too much additional clock skew to the timing margin of the design. With the increase of system clock frequency, there is also less margin for error in signal timing in order to meet reduced setup and hold time requirements. Noise problems resulting from transmission line effects include reflection noise, crosstalk noise, and power/ground switching noise (for more detailed information, see the Howard Johnson and Martin Graham book in the References list, page 27). These noise problems can lead to significant distortion of the digital signal waveforms. If the distortion is bad enough to exceed the noise margin of the logic devices, then signal errors will be introduced and the design will fail. Figure 1 shows an example of ringing that might be seen on a high performance digital signal and could be caused by any one of the signal integrity noise sources mentioned. The signal in Figure 1 is a 62 MHz PECL clock signal that has been badly misterminated. Note that the ringing on the falling edge of the signal occurs at the logic threshold and would probably result in incorrect clocking on that falling edge. Unfortunately, the ringing in Figure 1 could also be an artifact introduced by inadequate measurement equipment performance or probing technique. Understanding the possible causes of this type of noise is important in isolating and eliminating the true problem.

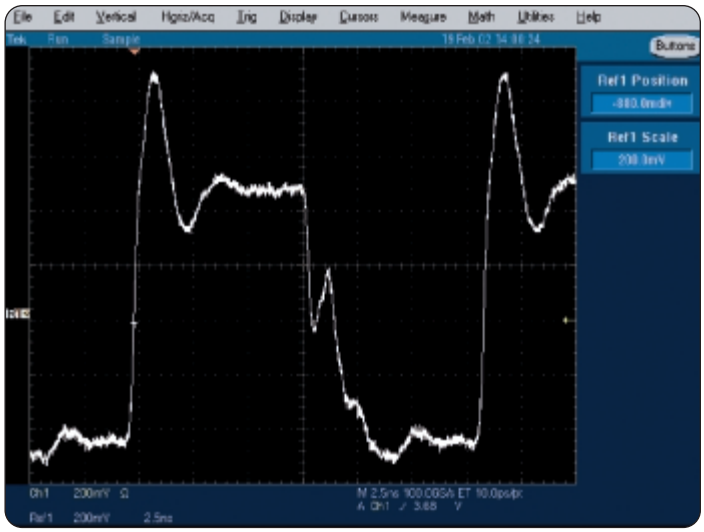


Figure 1. *Ringing caused by misterminated interconnect.*

Reflection Noise

One of the key parameters of a transmission line interconnect is characteristic impedance. Reflection noise results from discontinuities in impedance seen by a signal as it propagates along the interconnect path. These discontinuities in impedance can occur at the signal source, from variations of characteristic impedance along the interconnect path due to a variety of causes, or from impedance mismatch at the termination end of the signal path. Causes of characteristic impedance variations along the interconnect path include discontinuities due to stubs or branching of the signal path, load variations due to signal pickoff points along the line, path routing through vias or on different circuit board layers, or from discontinuities in the AC current return path. The resulting reflection noise can lead to increased time delay, ringing at signal transitions, and excessive overshoot and undershoot. Remedies for reflection noise include a variety of transmission line termination techniques, signal buffering for point-to-point connections, daisy-chain routing rather than branching, and the use of a continuous transmission line reference plane for a clean return current path.

Crosstalk Noise

Crosstalk noise results from electromagnetic coupling of signals between transmission line traces. Modeling of crosstalk using lumped circuit analysis is done with both mutual inductance and mutual capacitance. These effects are dependent on the rate of change of the signal and are thus more significant in high-speed designs. From the view of transmission line theory, coupling between two or more transmission lines causes change to the characteristic impedance and propagation delay of the affected lines. This same transmission line coupling also leads to crosstalk effects, where a signal present on one line can couple a portion of its energy to an adjacent line. Crosstalk noise, like reflection noise, is affected by signal rise time, line length, terminations, and return path continuity, but is additionally affected by line spacing and trace orientation. Because of the coupling of noise from an “aggressor” line to a “victim” line, error signals can occur on otherwise quiet signal traces. Because of the combination of mutual inductance and mutual capacitance effects, the crosstalk noise induced is different at the near end and the far end of the “victim” line. Crosstalk noise is also sometimes difficult to troubleshoot because it is pattern dependent, and may only appear as an intermittent failure. Crosstalk effects are not all bad, however, since coupling is used to advantage with differential signaling, where two lines are intentionally routed close together and are driven by complementary signals. Remedies for crosstalk noise include adding additional spacing between traces, minimizing the routing of parallel traces for long distances, adding ground guard banding between signal lines, and using differential signaling for critical signals.

Power/Ground Switching Noise

Power/ground switching noise results from transient currents in the power distribution network that produce voltage fluctuations in both the power and ground planes. Since the ground plane is generally used as the reference for the input threshold of digital receivers, current transients that affect the ground potential can lead to an effective shift in the input threshold. This voltage shift appears as an additional noise source that contributes to possible signal errors. Although bypass capacitors are usually distributed across a circuit board to try to localize the effect of current transients, their size, distribution pattern relative to the source of large current transients, and the inductance in the bypass capacitor routing path determine the amount of glitching seen in the power/ground network. The speed of the current transients also has an impact on the effectiveness of a discrete bypass capacitor network, and for the fastest transients, the parasitic bypass capacitor formed between the power and ground planes of a multilayer circuit board is probably the most effective. One type of power/ground switching noise is referred to as simultaneous switching noise (SSN), or ground bounce, and is caused by multiple output drivers switching state at the same time. The effects of SSN can be seen at not only the board level but also at the chip level, where inductance in the packaging of the device contributes to the problem. SSN is also a pattern-dependent noise problem, which may be difficult to troubleshoot because of its intermittent nature. Remedies to power/ground switching noise include care in the placement of bypass capacitors near IC package pins with minimum parasitic inductance; the use of full power and ground planes placed next to each other in a multilayer circuit board topology; care in the pin selection of programmable ICs or ASICs to ensure an adequate number of power and ground pins; similar care in the placement of pins for output drivers to spread out the effect of driver transients; and the use of differential signaling for critical signals.

Signal integrity noise problems, like those just mentioned, must be addressed by careful circuit board layout techniques. Many years ago, before the availability of sophisticated computer tools for circuit board layout, all circuit boards were routed by hand. Since the edge rates of devices at that time were orders of magnitude slower than those available today and the density of circuitry on the boards was much less than that seen today, signal integrity problems were generally not an issue. The introduction of the first auto routing layout tools for circuit board design were developed to improve the efficiency of the board design process. The results of these early tools, while certainly quicker than hand layout, often created very long and convoluted routing paths that required a thorough post-processing review and selective re-routing in order to avoid potential signal integrity problems. As digital system edge speeds increased and these signal integrity problems began to impact more digital designs, improved routing tools were designed to deal with these new signal integrity problems. The first of these improved auto routing tools for circuit board layout included the capability to constrain the layout design with physical design rules. These physical design rules, both global and net-specific, allowed the specification of such physical attributes as maximum trace delay, maximum stub length, maximum trace-to-trace parallelism, and maximum length to a termination resistor. Routing with physical design rules required the designer to translate electrical requirements into physical constraints, but was still a significant improvement over auto routing without constraints, which had to be followed by an extended post-processing review of the layout. Because of the increasing complexity of high performance designs, however, this post-processing layout review provided a great opportunity for missing potential signal integrity problems. The most recent improvement in circuit board design tools for high performance digital systems is the addition of electrical design rules based on signal integrity and timing analysis. The use of electrical design rules applied to the auto routing of a circuit board relieves the designer of the need to convert the electrical requirements into physical constraints. This reduces the large simulation effort required to build the timing and noise budgets, since the signal integrity analysis is designed to handle that simulation process as part of the placement and routing process. Since these interconnect analysis design tools perform their analysis continually during the routing process rather than as a post-processing operation, fewer routing iterations should be required, and the detailed post-processing verification effort should be reduced.

Although the improvement in the capability of circuit board layout tools has helped to decrease the risk that high performance digital boards will fail due to signal integrity problems, it has not completely eliminated all signal integrity problems. Like any simulation tool, the signal integrity analysis-driven layout tools are only as good as the models that are used in the simulation. The signal integrity analysis tools generally use industry-standard IBIS (input/output buffer information specification) models in their interconnect analysis simulations. These behavioral models allow the representation of device driver I/V characteristics, rise and fall time characteristics, the presence of protection diode clamps, and packaging parasitics. The IBIS models used by the simulation tools should ideally represent the worst-case conditions for signal integrity analysis. If these models are derived from typical device measurements rather than from IC simulation data that includes worst-case process parameter variation, the resulting simulations will not represent the worst-case noise conditions. Similarly, the simulation of the circuit board environment will be based on trace width and dielectric layer thickness that will vary some due to normal circuit board manufacturing process variations. Because of these variables and other similar problems, there still remains a need to verify the signal integrity of critical signals on every high performance design. The measurement instruments used to physically verify the signal integrity of these critical signals must have the necessary performance to accurately view the waveform quality without excessively disturbing the waveform shape due to loading.

The Signal Fidelity Challenge—High Performance Probe Measurement Issues

The standard measurement tool for verifying the signal integrity of high performance designs is the time domain oscilloscope. One additional measurement tool that is critical for cleanly transferring the signal to be measured to the input channels of the oscilloscope is the oscilloscope probe. The ideal oscilloscope probe should not disturb the signal being measured and should faithfully duplicate the response of the signal present at the probe tip. For low frequency signals, it is possible to approach the performance of this ideal probe. There are also a variety of probe types available to meet different measurement application needs (see *ABCs of Probes* in the References list, page 27). For high performance measurements, the recommended probe type will generally be a high-speed active probe. For high performance signals, there are a number of complicating factors that can easily distort the response of the signal being measured, deviating from the ideal probe performance in both loading and fidelity of response. High performance probe measurements in this paper will be defined as those made on signals in a transmission line environment that require at least 1 GHz bandwidth. An understanding of the issues that follow is needed to preserve signal fidelity when making high performance measurements.

TekConnect: An Advanced Probe Interface for Signal Fidelity

Since the days of vacuum tube circuits, the traditional probe interface on the front panel of oscilloscopes has been the BNC connector. Even with the integration of probe power supplies and offset control into the TekProbe™ interface in the mid-1980s, the BNC remained the connector of choice for the measurement signal path. The TekConnect probe interface was recently developed to address the bandwidth limitation of the BNC connector and provide improved reliability and ease of use (see Figure A).

The maximum useable bandwidth of a high-quality BNC connector is about 4 GHz. Recognizing that market demand for measurement bandwidth above 4 GHz was increasing, the TekConnect probe interface was designed with a BMA connector. The BMA connector is a blind mate connector similar in size and performance to an SMA connector, but with a threadless outer ground connection. The BMA connector provides a 50 ohm coaxial interconnect that is capable of supporting quality electrical performance up to at least 18 GHz. The probe power and control signals in the TekConnect interface are supported with a spring-contact pin block in the TekConnect "bucket" side of the interface. The gold-plated spring-contact pins mate with gold-plated pads on a small circuit board on the TekConnect "nose" side of the interface.

▶ ***Figure A.*** *TekConnect probe interface.*

Probe Bandwidth/Rise Time

Probe bandwidth refers to the frequency response characteristic of a probe and specifies the normal operating frequency range of the probe. Since probes are used to connect a measured signal to the input of an oscilloscope, the system bandwidth of the probe and oscilloscope together is really more important than the probe-only bandwidth. If the measurement system bandwidth were infinite and its response were perfectly linear, it should be able to reproduce exactly any signal measured at the probe tip. A realistic measurement system with its limited bandwidth and imperfect response, however, will always produce a somewhat distorted representation of the real input signal. In order to try to minimize this distortion, it is recommended that the measurement bandwidth and rise time be three to five times faster than the signal to be measured. Because of the continuing market demand for higher measurement bandwidth, Tektronix has a high performance oscilloscope/probe interface called TekConnect (see TekConnect: An Advanced Probe Interface for Signal Fidelity, page 8).

Since oscilloscope probes are primarily used for time domain measurements, the probe rise time is often considered a more important specification than its bandwidth. In addition, since the probe bandwidth is inversely proportional to its rise time, the probe rise time is often a guaranteed specification while its bandwidth is often listed as a typical specification and may be calculated from the rise time-bandwidth product. The bandwidth of most high performance probes, however, is now verified directly during the manufacturing test process. The bandwidth-rise time product for most probes is a constant between 0.35 and 0.45, generally depending on the amount of peaking in the probe response. Since the oscilloscope that the probe is attached to has a finite rise time, the combined oscilloscope/probe system rise time should also be measured or calculated. An approximate equation for measurement system rise time is:

$$\text{Measurement system rise time} = \sqrt{(\text{oscilloscope rise time}^2 + \text{probe rise time}^2)}$$

Note that this approximate system rise time formula only applies to the cascading of non-interacting linear systems. Fortunately, the TekConnect

The TekConnect interface also features a convenient, positive-locking mechanical connection. The TekConnect probe or adapter attachment is made by pushing the nose piece into the bucket side of the interface. A spring-assisted pull-in force in the bucket side of the interface assures a reliable connection, and a lock mechanism in the interface nose piece retains the interface connection until intentionally released. Probe or adapter release is a single-hand operation in which the push- button lock release is pressed at the same time the probe or adapter is pulled out. In addition to enabling future extension of probe bandwidth to at least 18 GHz, the TekConnect interface provides some additional electrical and mechanical features that should please the most demanding customer.

Improved Oscilloscope/Probe Communication Capability

The previous generation TekProbe-BNC interface had an oscilloscope/probe communication protocol, but it was generally limited to read-only features such as probe-type identification, probe scale factor, probe dynamic range, probe offset range, etc. The TekConnect interface enables additional control features that allow for electronic calibration adjustments, soft switching of probe parameters, oscilloscope interrupt capability, and cascading of accessories (e.g. the TCA-1MEG 500 MHz buffer amplifier). One example of improved oscilloscope/probe communication capabilities with the TekConnect interface is the ability of some TekConnect oscilloscopes to boost the measurement system bandwidth when a probe is attached. For example, the P7240 probe-only bandwidth is 4 GHz and the TDS7404 scope input bandwidth is also 4 GHz. When a P7240 probe is attached to a TDS7404 input channel, the expected system bandwidth using the conventional technique for cascading two linear amplifiers is only about 2.8 GHz.

$$\text{Expected System Bandwidth} = 1/\sqrt{((1/4\ \text{GHz})^2 + (1/4\ \text{GHz})^2)} = 2.8\ \text{GHz}$$

interface has intelligent features that may improve system rise time when TekConnect probes are attached to TekConnect oscilloscopes. For best signal fidelity, it is normally recommended that measurement system rise time be three to five times faster than the signal to be measured. Since time domain instruments are usually characterized by the quality of their pulse response, a great deal of Tektronix' design effort is to not only maximize probe bandwidth, but also to minimize aberrations and irregularities in a probe's pulse response.

Probe Dynamic Range

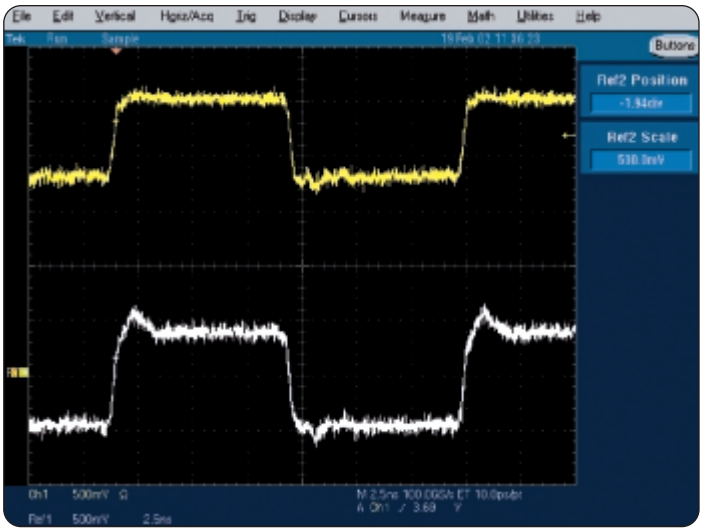
Dynamic range in active probes refers to the range of input voltage over which the probe provides a linear response. When a signal is applied to the probe input that exceeds its dynamic range, the signal output by the probe to the oscilloscope will be compressed. The signal compression that results from exceeding a probe's dynamic range can give a very inaccurately displayed response. An example of this problem is shown in Figure 2, where the same PECL signal is displayed, but with two different offset settings. The displayed PECL signal has a logic swing of about 1V peak-to-peak, balanced around its logic threshold level of +3.7V. The lower trace, with an offset of +3.7V, is fully within the ±2V dynamic range of the probe but the upper trace, with an offset of only +1.5V, is partly outside the dynamic range of the probe. The lower trace shows that the PECL signal has a noticeable reflection overshoot. In the upper trace, however, the same PECL signal is compressed by dynamic range limiting and appears to have a virtually flat response, with slight compression of its peak-to-peak amplitude. This erroneous response might cause the designer to incorrectly assume that his circuit was

Because of the intelligent bandwidth control capability of the TDS7404, the oscilloscope is able to read the probe-only bandwidth factor stored in the probe's internal EPROM and boost the measurement system bandwidth of the P7240 attached to the TDS7404 to about 4 GHz. Without the TekConnect communication protocol and the intelligent bandwidth control of the TDS7404 oscilloscope, this dramatic increase in system bandwidth would only be available with a oscilloscope having more than three times the bandwidth and the same probe bandwidth, or similarly with a probe having more than three times the bandwidth and the same scope bandwidth.

Improved Probe Interface Reliability

Both the electrical and mechanical reliability of the oscilloscope/probe interface has been improved with the TekConnect design. This improved reliability has been confirmed by extensive environmental testing of the TekConnect interface. The electrical interface in the TekConnect design includes both the RF signal connector and the power/control pins. The use of high-quality BMA mating connectors and a careful mechanical design that supports the tolerance requirements of a threadless connector interface have been shown to support thousands of insertion cycles reliably. The spring-contact pins used in the probe power/control interface pin block are standard, high-volume process components and have also been tested for thousands of insertion cycles with negligible contact resistance increase. The placement of the spring-contact pin block in the recessed cavity, or "bucket" side, of the TekConnect interface protects the pins from damage, which should be more reliable than the exposed pin design of the older TekProbe interface. The reliability of the probe power pins in the TekConnect interface has also been improved by using an interconnect protocol that only switches power to the pins when a valid probe connection has been detected. This reduces the risk of contact damage or degradation to the probe power

performing well, when in reality there may be serious problems that are masked by the probe's dynamic range limitation (see Active Probe Dynamic Range and Offset, page 12).



▶ ***Figure 2.*** *Example of signal compression (top trace) caused by exceeding the dynamic range.*

pins caused by high inrush currents. Extensive test cycling and environmental testing of the TekConnect interface has confirmed the improved reliability of switched probe power pins.

Improved Interface Flexibility with TekConnect Adapters

The availability of a variety of 50 ohm input connectors for the TekConnect interface provides a new level of flexibility and convenience. High bandwidth SMA and N-type adapters are available, along with a more traditional BNC adapter. Since the TCA-BNC adapter provides only a 50 ohm input to the high performance TekConnect vertical channels, a new TCA-1MEG buffer amplifier is also available to provide a more conventional high-impedance BNC input. A new and expanding line of TekConnect probes, which presently includes the P7240, a 4 GHz single-ended active probe, the P7330, a 3.5 GHz differential probe, and the P7260, a new 6 GHz single-ended active probe, is also available with the same easy-to-use TekConnect interface. The use of TekConnect interface adapters, rather than fixed front panel connectors, provides a flexible way of configuring a TekConnect oscilloscope with a front panel connector set that meets the needs of different applications. The TekConnect interface allows for easy swapping of probes and adapters with changing application demands. The use of TekConnect interface adapters, rather than fixed front panel connectors, also provides a relatively inexpensive and convenient means for connector replacement in high-volume usage situations, such as manufacturing test applications.

Probe Loading

When a probe is connected to a measurement node, it provides some parasitic loading of the signal being measured. This parasitic loading will result in degraded signal integrity and signal fidelity. Depending on the frequency content of the signal, the source impedance of the measurement node, and the degree of parasitic loading, the measured waveform may be significantly distorted or not. Also, depending on the sensitivity of the measurement node to loading, the circuit function itself may be affected. Most probes provide some specification of both DC and AC loading. The DC loading specification for the P7240, 4 GHz TekConnect active probe is 20 kohm input resistance. The AC loading specification for the P7240 is 1 pF input capacitance. This probe is designed with a 5X input attenuator on the probe tip hybrid. The use of an input attenuator and other careful design techniques were employed to try to control and minimize the input capacitance since it has such a dramatic loading effect on high frequency signals. In a high performance probing situation, the effect of probe capacitance loading can lead to additional delay in the signal path as well as increased transmission line reflection problems. Because of input capacitance loading, the profile of the input impedance magnitude with frequency for the P7240 drops from 20 kohm at DC to a calculated value of 160 ohms at 1 GHz. This calculated value of impedance is not entirely realistic, however, since frequencies of 1 GHz and above the load impedance may also be significantly affected by the inductance of both the probe tip and ground lead connections. As shown in the modeling section of this paper, a more complete probe load model should include transmission line elements and will require variations with different ground lead connections.

Active Probe Dynamic Range and Offset

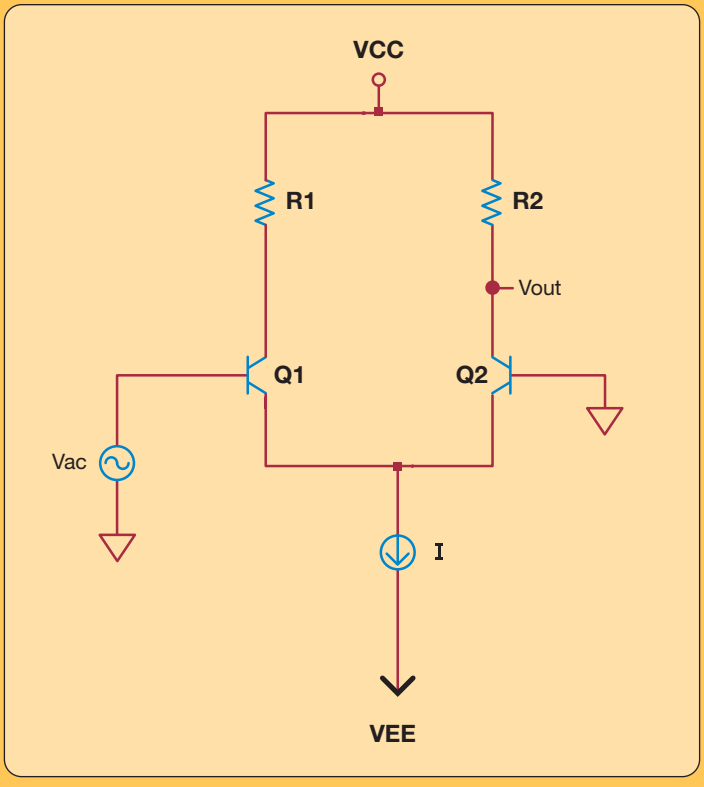
Probe dynamic range has become a much more important issue in recent years because of the demand for higher probe bandwidth and reduced probe loading. These performance demands have forced an evolution in probe technology, from passive to active designs. With passive probe designs, dynamic range is generally not an issue since the limiting factor in passive probe dynamic range is the maximum voltage rating of the probe, which is usually several hundred volts. The use of high impedance passive probes is instead limited by bandwidth (≤ 500 MHz) and input capacitance loading (≥ 8 pF). Active probe designs use a buffer amplifier in the probe tip to extend the probe bandwidth and reduce the input capacitance. The active probe buffer amplifier also provides a 50 ohm output driver stage to pass the input signal down the probe cable to the oscilloscope with minimum distortion. Active probe designs require the user to deal with the dynamic range limitation that results from the use of a buffer amplifier.

With increasing bandwidth demand, active probe designs have been forced to require more limited dynamic range. As the migration of integrated circuit technology to smaller line widths has resulted in faster, but smaller, logic swings, a similar evolution in probe amplifier technology has resulted in faster response, but more limited dynamic range. The dynamic range in earlier generations of active probes tended to be limited by the available probe power supplies to ± 8 to 10V. More recent higher performance probes have been forced to limit the probe dynamic range to ± 2V in order to maximize the probe bandwidth. Although a wider dynamic range would be more convenient for the user, the required dynamic range to meet the needs of today's high performance measurements has also decreased because of high performance IC process limitations. Fortunately, the faster signals in today's high performance measurement applications tend to also have a smaller signal swing. Note that the effective input voltage range of an active probe may be wider than its dynamic range if it has a probe offset control capability. For most high performance logic families, to utilize a single-ended power supply, the normal logic signal swing is not centered around ground. However, since the probe dynamic range is centered around ground, a probe offset control is included to try to extend the effective dynamic range of these active probes. An example of the use of probe offset control will be given at the end of this section.

An example of the variation of probe loading with two different probes will now be shown on a high-speed digital communications signal. The probes compared are differential probes, since a differential signal input is to be measured. The two differential probes are a P6248 probe with 1.7 GHz bandwidth and < 1pF differential input capacitance and a P7330 probe with a 3.5 GHz bandwidth and < 0.5pF differential input capacitance. The input signal that was applied to a differential microstrip feedthrough test fixture was a 1.5 Gb/s pseudo-random data pattern with a 40 ps rise time. By using a feedthrough test fixture, it is possible to see both the measurement signal response of the probe as well as the effect of the probe loading on the measured signal. Probing the signal on the test fixture's differential microstrip transmission lines allows the measured signal response to be observed. At the same time, the probe loading effect can be seen by looking at the feedthrough outputs from the test fixture with a differential sampling head. The results of the test are shown in Figures 3, 4, 5 and 6. Figure 3 shows the input signal from the pattern generator measured at the feedthrough outputs of the test fixture with no probe loading. The top trace of Figure 4 shows the same input signal as Figure 3, but slightly distorted because of the

▶ ***Figure 3.*** *1.5 Gb/s signal with no probe loading.*

effect of the P7330 probe loading on the microstrip transmission lines. The bottom trace of Figure 4 shows the P7330 response to probing the digital communication signal on the test fixture microstrip lines. The top trace of Figure 5 shows the effect of probe loading on the same input signal with the lower performance P6248 probe. The significantly



▶ ***Figure B.*** *Simple differential amplifier.*

The primary building block of integrated linear amplifier technology is the differential amplifier stage (see Figure B). The exponential transconductance characteristic of bipolar transistors results in a highly nonlinear response for this differential amplifier topology. The nonlinear characteristic of the bipolar differential amplifier provides a natural limiting action. ECL logic circuits, which utilize this same differential amplifier topology as a logic comparator, use this nonlinear limiting action to set the limits of the ECL logic swing. When driven by an input differential voltage signal, the linear dynamic range of this simple differential amplifier is only about 50 mV peak-to-peak. By the time the input signal has reached 200 mV peak-to-peak, the differential amplifier is fully limited and all of the current into the coupled emitter current source flows through only one of the two differential transistors. Feedback techniques are usually used to extend the linear dynamic range of an amplifier beyond the very limited range of a simple differential amplifier stage. The dynamic range of a high performance amplifier, such as a probe buffer amplifier, must still be limited, however, in order to meet linearity, bandwidth and power dissipation requirements.

increased signal distortion due to the heavier loading by the lower performance probe should be evident. The middle trace of Figure 5 also shows the P6248 response to probing the digital communication signal on the test fixture microstrip lines. The inability of the lower speed P6248 probe to respond accurately to a signal beyond its effective measurement range should also be evident. Figure 6 shows the effect of loading the microstrip lines on the test fixture with both the P7330 and P6248 probes at the same time. Note that the dominant loading effect still comes from the higher capacitance P6248 probe and that the higher performance P7330 probe is able to accurately respond to the distortion of the input signal caused by that probe loading. In general, a probe with higher bandwidth performance will exhibit less probe loading effect on a high-speed signal. It should also be noted that the probe loading distortion of the P6248 probe would be reduced significantly for slower input signals, such as a rise time greater than the 265 ps rise time specified for the probe.

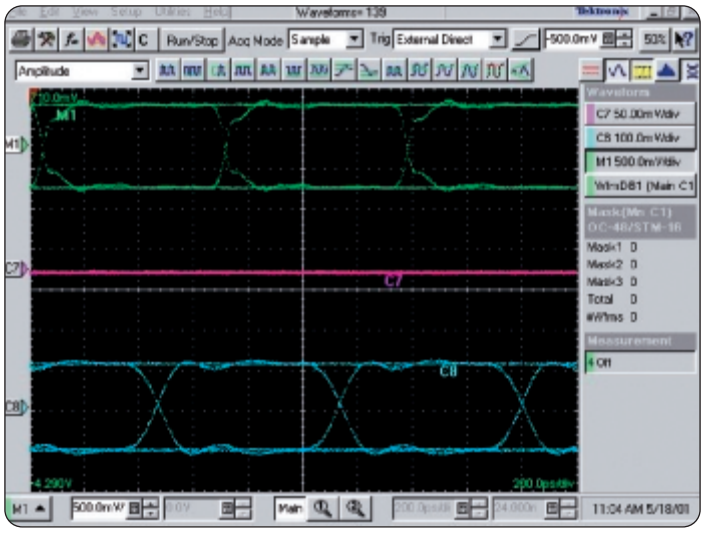


Figure 4. *1.5 Gb/s signal loaded by P7330 differential probe.*

The P7240, a 4 GHz active probe, is an example of a high performance probe with the dynamic range limitation and offset control that have been mentioned. A simplified schematic diagram of the P7240 is shown in Figure C. The probe head contains a 5X resistive input attenuator and the probe tip buffer amplifier. The offset control uses the 20 Kohm resistive attenuator as a summing junction for the input signal and the DC control signal from the offset amplifier. The offset signal is used to cancel out the effect of a DC common mode component of the input signal by applying a DC voltage of the opposite polarity. The probe cable contains both the 50 ohm signal coax as well as tiny messenger wires that bring power and the DC offset control signal to the probe tip amplifier. The probe compensation box contains a calibrated offset amplifier and some miscellaneous probe status/control circuitry. Both the probe tip buffer amplifier and the calibrated offset amplifier are designed for approximate unity voltage gain. The gain of the probe tip buffer amplifier is calibrated with the input attenuator to give a 5x attenuation for the input signal path. The offset amplifier is then calibrated with the input attenuator and probe tip buffer amplifier to give a 1x gain for the offset signal path. This gain ratio between the input and offset

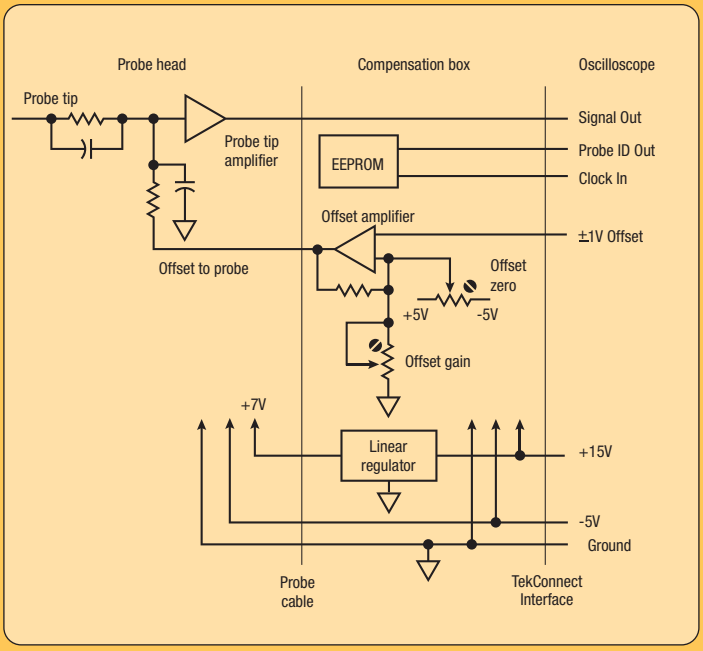
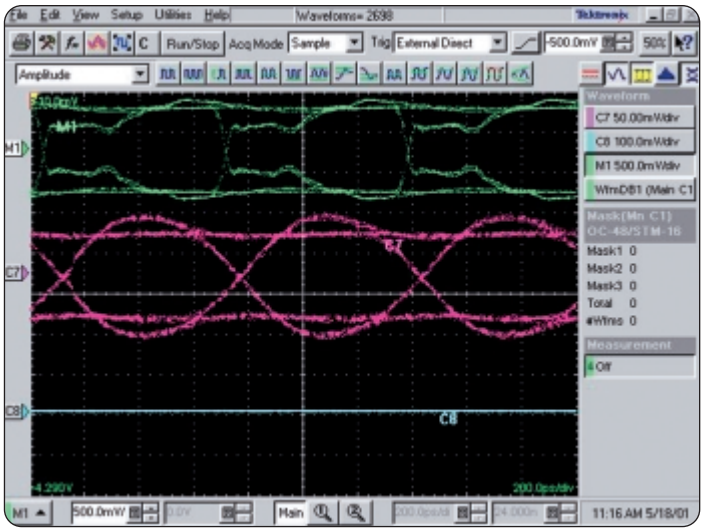
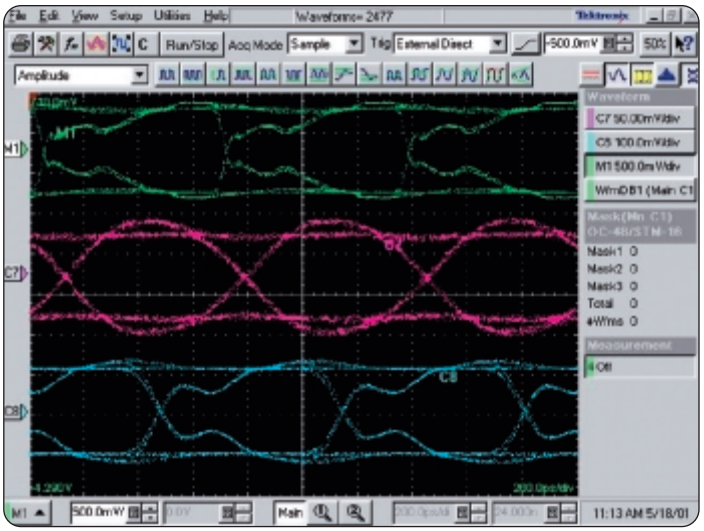


Figure C. *P7240 offset control circuit.*



▶ ***Figure 5.*** *1.5 Gb/s signal loaded by P6248 differential probe.*



▶ ***Figure 6.*** *1.5 Gb/s signal loaded by P6248 and P7330.*

signal paths causes an effective 5X multiplication of the ±1V offset signal from the oscilloscope. This results in a ±5V offset range referred to the probe input. The use of the offset control allows the 4V peak-to-peak dynamic range of the P7240 probe buffer amplifier to be moved up and down within a ±7V operating range window. Status information supplied from the P7240 probe to the oscilloscope over the TekConnect interface allows the oscilloscope to scale the offset signal so that the offset is displayed in volts referred to the probe input.

Knowledge of the expected voltage range of the signal to be measured is important for effective use of a high performance probe like the P7240. For example, consider the probe setup for measuring a PECL logic signal. Although the PECL signal logic swing of about 800mV peak-to-peak is well within the dynamic range of the P7240, the PECL threshold voltage of +3.7V requires that the P7240 offset be adjusted to place the PECL signal within the dynamic range of the P7240. If the probe offset were left at the default setting of 0V, only a small portion of the PECL signal would be displayed and the signal would be highly compressed. The best performance of the P7240 probe can be expected when the probe offset is set to the +3.7V PECL threshold level. (Oscilloscope vertical offset is different than vertical position: the vertical position control is used to adjust the relative placement of channels on the oscilloscope display; the vertical offset control is used to compensate for DC common mode voltage at the probe input.) Many Tektronix oscilloscopes, particularly those with the new TekConnect interface, now read dynamic range information from the probe and display the probe dynamic range window on the screen briefly when a vertical adjustment such as offset, scale, or position is made on the probe's channel. If available, this dynamic range limit display can be helpful in determining the linear range of a probe measurement and in setting the offset control to an optimum value.

Probe Grounding

A single-ended probe such as the P7240 requires a ground return connection in order to complete the measurement circuit current path. The P7240 probe has a ground socket connection that mounts on the back of the probe tip hybrid. Connection of various ground lead adapters to this socket provides some flexibility in making a ground connection to the circuit to be measured. The length of this ground return path in the probe measurement circuit can, however, be critical in high performance probe measurements. The length of the ground lead connection contributes directly to parasitic inductance in the probe input circuit (see Figure 7). The probe ground lead introduces about 20 nH/inch of inductance into the ground lead return path. This parasitic inductance forms a resonant circuit with the probe input capacitance that can lead to undesirable ringing, particularly when driven by a low impedance source. Figure 7 also shows a damping resistor in the probe input circuit, which is included in the probe circuitry to try to minimize the effects of the resonant circuit formed by the probe and its measurement environment. This damping resistor is usually chosen to damp the minimum probe inductance configuration in order to maximize the probe frequency response. As a general rule, the probe ground lead should be made as short as possible in order to minimize this parasitic inductance. This should not imply, however, that probe ground lead length should be minimized by increasing probe tip length. It has been observed that for most active probes, tip lead length causes more signal distortion than an equal ground lead length. Where possible, ground pads or vias should be designed into the circuit board around critical measurement nodes, preferably with the signal-to-ground spacing that matches the probe being used (note that this is typically 0.1 inch spacing). Minimizing the ground lead inductance does not eliminate the parasitic resonant circuit, but does minimize its impact by moving the resonant frequency up beyond the response range of the probe and signal source. Another good reason for minimizing both the ground lead length and its loop area is to minimize noise pickup by the ground lead loop. In high performance digital designs this induced noise results primarily from mutual inductance coupling effects and can be reduced significantly by minimizing the ground lead loop area.

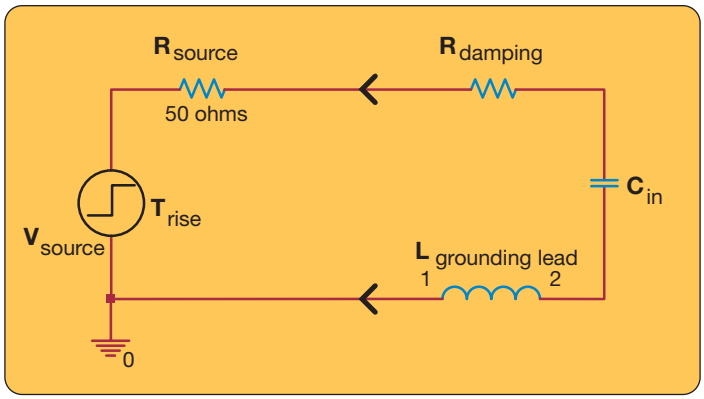


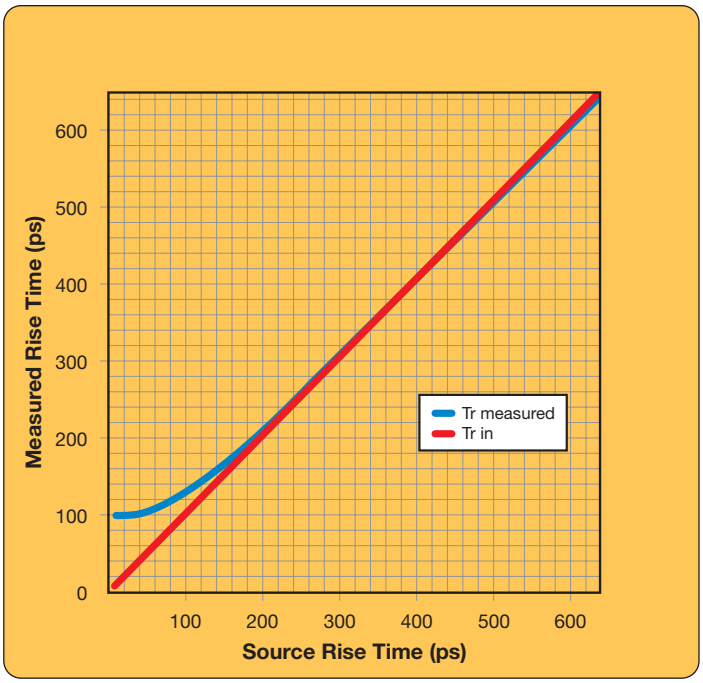
Figure 7. *Simplified probe loading model.*

Probe Resonant Effects

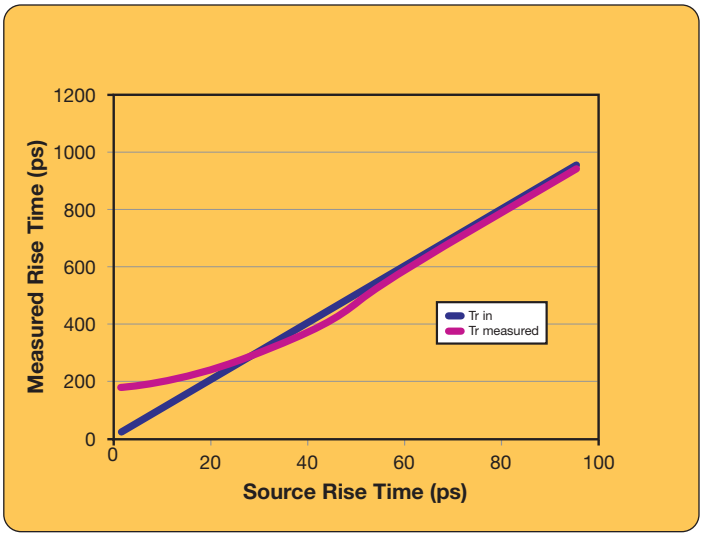
One consequence of the RLC circuit formed by the probe input impedance is the possibility of resonant effects that can distort the measured signal. The capacitance of a single-ended active probe input includes contributions from the input capacitance of the custom ASIC, the routing capacitance of the probe hybrid circuit, and the capacitance of the probe tip, including any parasitic capacitance from probe connection adapters. The inductance of a single-ended active probe input includes contributions from the probe tip signal path and probe ground path in the probe head structure and potentially much larger contributions from ground lead adapters that are needed to locate a local ground connection. Although a damping resistor is included in the probe hybrid circuit to control pulse response aberrations, the damping resistor value is usually chosen for use with a minimum ground lead inductance in order to maximize probe frequency response. The frequency response peaking of the probe input RLC circuit acts to distort the desired flat frequency response of a measurement tool. In order to minimize this distortion effect, it is highly desirable to try to move the LC resonant frequency of a probe out beyond either the frequency range of the signal input or the response range of the probe. Reducing the probe input capacitance and input inductance will increase the probe LC resonant frequency. The probe input capacitance can generally be reduced only by changing to a higher performance probe. The probe input inductance can be reduced only by minimizing the tip and ground lead length. For accurate high performance measurements, the highest performance probe available should be used and the shortest tip and ground lead length should always be chosen. Although probe adapters with relatively long tip or ground leads are usually available for high performance probes, they are included for application flexibility when

measuring lower frequency signals. For high performance measurements, long adapters need to be used with great care and with an understanding that they can degrade signal fidelity when measuring high speed signals.

An interesting example of probe resonant effects can be seen when attempts are made to try to measure signals that are close to or beyond the specified frequency range of a probe. It is generally expected that the frequency response of a probe will be relatively flat throughout its normal operating frequency range and will then roll off smoothly beyond its specified bandwidth. Although this may be true of a probe that is being used with minimum input inductance, it is not necessarily true for probes with much larger input inductance, due for example, to the use of a "long" ground lead (note that "long" for high performance probes may be an inch or less). This normal frequency roll off characteristic would ordinarily lead to a lower limit to the measured rise time of a signal as the rise time of the signal decreases. Figure 8 is an example of this effect for a P7240 probe with a specified rise time of <120 ps in a minimum inductance configuration. The close tracking of the measured rise time to the input rise time for slower input rise times is evident down to an input rise time of about 200 ps. The lower limit to the measured probe rise time of about 100 ps is also clearly visible in this figure as the source rise time continues to decrease below 200 ps. Because of probe resonant effects seen with non-minimum ground lead inductance, it is possible to observe an "inversion" region near the measurable rise time limit of a probe's response, where a rise time faster than the input rise time can be apparently measured. Figure 9 is an example of this effect for a P7240 probe like that in Figure 8, but with an additional 5nH (about 1/4 inch) of ground lead inductance. The presence of the "inversion region" where the measured rise time is less than the input rise time can be seen in this figure and is an artifact of the input resonant circuit. With larger tip or ground lead inductance this effect becomes even more pronounced and can even make a probe with a lower bandwidth specification appear to measure a faster rise time than a higher performance probe. Although not a common situation, this non-intuitive response can be avoided by always using the shortest ground lead length possible and not using probes beyond their specified range of operation.



▶ ***Figure 8.*** *DUT (Actual) vs. Measured Rise Time.*



▶ ***Figure 9.*** *DUT (Actual) vs. Measured Rise Time showing the inversion region.*

The Circuit Simulation Challenge— High Performance Modeling Issues

The high performance design issues that were addressed in the previous section on signal integrity described transmission line effects that could lead to circuit failures unless careful circuit layout techniques are employed. The choices made in component placement and signal routing as well as the circuit board layup for power and ground layer distribution can make or break many of today's high performance designs. Problems with individual signal reflection noise, crosstalk noise from signal-to-signal interaction, and the combined contribution to power/ground noise of many switching signals can lead to unanticipated design failure. The often intermittent nature of signal integrity problems in which design failures occur only at seemingly random times causes frustration for designers and demands methods to deal with the problem.

One method that has been employed with some success in high performance designs is the use of design guidelines for circuit board layout. The problem of reflection noise is often addressed by setting limitations on the routing length of signal traces or, where that is not possible, by the use of signal termination techniques when a trace delay exceeds some fraction of the signal rise time. The problem of crosstalk noise is similarly addressed by setting restrictions on trace-to-trace spacing and limitations on the parallel routing distance of non-differential signals. Crosstalk problems between circuit boards can also be reduced by design guidelines on the signal and ground pin distribution on board interface connectors. The problem of power/ground switching noise can be minimized by following design guidelines on bypass capacitor placement and the use of multi-layer circuit boards with power and ground plane layers.

Although the use of design guidelines can be a great help in minimizing signal integrity problems, relying on them without understanding the underlying principles can lead to problems. The complexity of the design environment and the increasing speed of today's high performance designs has led to the need for simulation tools that attempt to model the design by extracting information from the circuit board layout and the component model database. Layout simulation tools can provide insight into the performance of a design and can help pinpoint potential signal integrity noise problems. Integrating layout simulation tools with circuit board layout tools allows the circuit designer to place constraints on trace routing and speed up the design process. By helping to locate potential problems before a design is physically built, simulation tools can also reduce the time to market, and pay back the tool cost and the time needed to become proficient in the use of a simulation tool.For those unable to afford the cost of an embedded layout simulation tool or where simulation of only a few selected signal paths is needed, the use of a traditional analog simulation tool, like Spice, can be very useful in modeling the routing of transmission lines. The routing of a synchronous clock signal is an example of a situation where simulation might be useful to analyze signal integrity problems. Because of its global nature, a synchronous clock signal often has a long routing path, a heavy capacitive load because of multiple connections, and is sensitive to reflections since signal ringing that exceeds the logic threshold can cause double clocking and almost certain circuit failure. Depending on the details of the routing path and the rise time of the clock signal, the simulated clock waveform may appear to have a significantly different shape at different points in the routing path because of transmission line effects. Assuming that the Spice model extracted by hand from the preliminary layout accurately includes the effect of trace lengths, trace characteristic impedance, parasitic stubs, IC pin loading, and possibly more subtle effects like vias or other trace discontinuities, the problem of transmission line ringing should be controllable. Transmission line ringing should be predictable from the physical layout of the interconnect path and the characteristics of the driving signal and, once the effects are understood, ringing should be able to be minimized by either trace layout changes or with the addition of signal termination techniques that attempt to control the transmission line environment.

The accuracy of a design simulation is only as good, however, as the accuracy of the models used. Accurate simulation of individual transmission line effects requires good modeling of the signal driver, the routing topology and characteristic impedance of the interconnect, and the loading effects caused by any receivers. Modeling of the signal driver requires knowledge of both driver output impedance and signal swing as well as the signal rise and fall times. Modeling of the signal interconnect requires knowledge of the routing path, including the trace length of each branch the signal follows. The characteristic impedance of the interconnect must also be modeled, which for microstrip lines requires knowledge of trace width, the circuit board material dielectric constant, and the thickness of the dielectric layer between the signal trace and its reference plane. Modeling of receiver loading requires knowledge of the input capacitance of each receiver and its location along the signal routing path as well as any transmission line terminations that may have been added to control signal integrity noise problems.

The accuracy of the simulation models for a transmission line simulation are dependent on the actual characteristics of the driver and receiver ICs and the construction of the circuit board. Measurement techniques can be used to characterize the interconnect quality and verify how well the simulation matches reality. Variations in the circuit board construction process can affect all the variables that contribute to the actual characteristic impedance: the width of the trace, the circuit board dielectric constant, and the thickness of the dielectric layer. The characteristic impedance of the signal interconnect can be measured using TDR techniques. Although TDR probes can be used to verify the performance of almost any signal path on a board, it is often easier to verify the overall board impedance design with a test coupon that has a more controlled trace access connection. The characteristics of the driver and receivers are affected by integrated circuit process variations, which may cause variations in the signal rise time by as much as a factor of two or three. The driver rise time used in the simulation model may not be the fastest rise time expected from normal IC process variations, which is the worst case value for signal integrity noise. If the slowest rise time expected from normal IC process variations is used instead in the simulation model, then the resulting simulation results may appear very good, but will give an accurate representation of possible problems. Measurement of actual signal performance should be made with high performance oscilloscopes and probes in order to verify the accuracy of the driver and receiver simulation models. Understanding the issues discussed in the previous section on signal fidelity and the models described in the following sections can be used to improve both signal interconnect simulations as well as verification measurement.

TekConnect Probe Modeling— Test Fixtures and Modeling Techniques

The Spice models developed for the TekConnect probe in this paper are designed to provide both probe load modeling information as well as probe response modeling information. Probe load modeling information was extracted from both TDR measurements and TDT measurements on a custom test fixture (see Figure 10). The custom test fixture was designed as an open metal housing with input and output SMA launch connectors both attached internally to a grounded coplanar waveguide. The grounded coplanar waveguide structure looks like a microstrip transmission line with top-side ground fill. A coplanar waveguide structure was chosen for the transmission line rather than a simpler microstrip structure in order to provide a low inductance probe ground connection. The grounded coplanar waveguide circuit board was constructed of a low-loss dielectric material for the most accurate high performance measurements. The test fixture was designed for use in both single-ended and differential active probe performance testing.

The measurement system included the custom test fixture and a high bandwidth, low noise sampling oscilloscope. The oscilloscope sampling head featured 20 GHz bandwidth and included a TDR pulse source with about a 25 ps rise time. The measurement system was configured with the sampling head TDR channel driving one SMA connector of the custom test fixture and the TDT measurement channel attached to the other SMA connector. By pressing the probe head against the middle of the test fixture transmission line, the loading of the probe could be observed both on the TDR impedance response as well as on the TDT pulse response. On the TDR response waveform, the probe loading appears as a capacitive dip in the flat section of the impedance profile that represents the 50 ohm characteristic impedance of the test fixture. By integrating the area of the capacitive dip on the TDR response, it is possible to extract the value of the probe input capacitance. On the TDT response waveform, the probe load appears as an aberration in the pulse response that is transmitted through the test fixture transmission line. The rise time of the TDR pulse signal at the TDT measurement port is also slowed somewhat due to the probe loading.

Probe response modeling information was extracted from the same measurement system configuration by measuring the probe response to the TDR pulse stimulus with the probe placed at the middle of the test fixture transmission line. Although a TekConnect probe is designed for plugging into a TekConnect oscilloscope with its response then becoming part of the oscilloscope/probe system response, it is possible to independently measure the probe response using another special test fixture. By using a TekConnect Calibration Adapter, a TekConnect probe can be powered from a TekConnect oscilloscope and its direct output response can be measured with a high bandwidth sampling oscilloscope on the TekConnect Calibration Adapter SMA output connector. With a 50 ohm pulse source impedance and a 50 ohm sampling head termination impedance, the effective source impedance seen by the probe in this measurement system is 25 ohms, which is the normal impedance environment used when measuring probe performance. Probe rise time and aberrations were measured with the measurement system just described; probe bandwidth was measured with a network analyzer and the same custom test fixture.

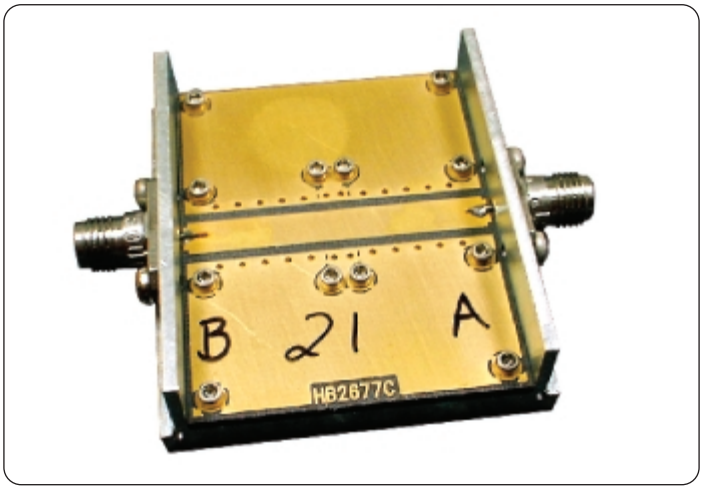


Figure 10. *Custom probe test fixture.*

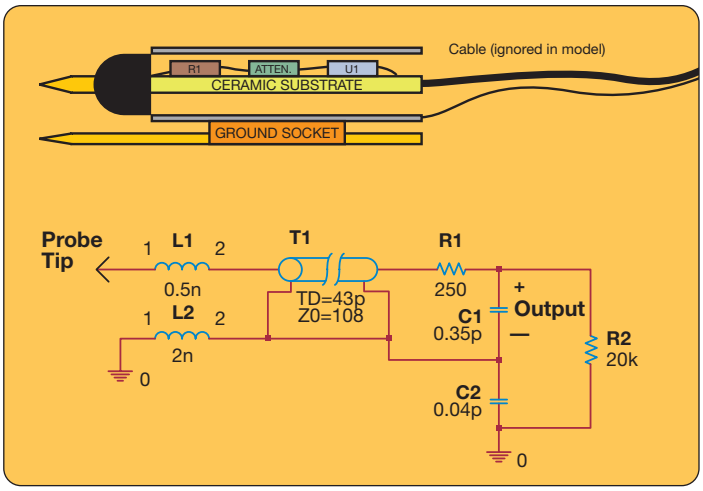
A TekConnect Probe Modeling Example: The P7240 Single-ended Active Probe

The P7240 is a 4 GHz, single-ended active probe featuring the new TekConnect interface. The high performance and small profile probe head of the P7240 results from the use of hybrid circuit technology and a custom ASIC. The key performance specifications for the P7240 are listed in Table 1.

The key performance specifications of the P7240 include both probe loading characteristics as well as probe measurement performance characteristics. The P7240 Spice modeling has been developed with the goal of including both probe loading effects as well as probe measurement performance in a combined model. It is very important to recognize that both the probe loading and probe performance characteristics of a high performance probe like the P7240 are significantly affected by the probe attachment environment. The P7240 key performance specifications listed in the table below only apply for the case of minimum probe tip and ground lead inductance. The P7240 is tested in manufacturing with a special minimum inductance test fixture. Since the P7240 probe tip and ground connections are both supplied with sockets, the minimum probe tip inductance modeling case implies no probe tip accessory in the probe tip socket and a very short ground lead pin in the probe ground socket. When a probe tip or longer probe ground pins or leads are added, the P7240 performance will be degraded and the probe's Spice model must be modified. Three P7240 modeling cases will be considered in this paper:

- P7240 with no adapters
- P7240 with probe tip and pogo ground pin
- P7240 with probe tip and 3-inch ground lead

The Spice models of the P7240 probe have been fitted to measurement results rather than being fully extracted from the physical structure of the probe design. This has been done in order to produce as simple a set of models as possible that still matches the probe measurement results. For the P7240 modeling cases to be presented, the models are case-specific, rather than modular. The addition of a different probe tip and ground lead adapters resulted in changes both to the model component values as well as some additions to the basic model topology.



▶ ***Figure 11.*** *P7240 model with a very short ground.*

Although the Spice models of the P7240 probe have been fitted to measurement results rather than being fully extracted from the physical structure, there is a noticeable relationship between the P7240 Spice model and the physical construction of the probe head assembly. Figure 11 shows a composite of the Spice model for the case of a P7240 with no adapters along with a simplified drawing of the P7240 probe head assembly. In the P7240 Spice model in Figure 11, the model inductor L1 represents the inductance of the P7240 probe tip socket. Similarly, model inductor L2 represents the P7240 probe ground socket and pin inductance. The model transmission line T1 can be considered to represent the signal path from the probe tip to U1, the ASIC buffer amp. A transmission line was chosen to represent this signal path rather than a lumped LC circuit because it seems to reflect the physical reality better for a high performance probe like the P7240. The model damping resistor R1 is included in the probe signal path to represent the damping resistance that is included in the P7240 hybrid

Bandwidth	DC to 4.0 GHz (typical)
Rise Time	< 120 ps (guaranteed)
Attenuation	5X
Dynamic Range	± 2.0V
DC Offset Range	± 5V
Input Resistance	20 kohm (typical)
Input Capacitance	< 1pF (typical)

▶ ***Table 1.*** *P7240 key performance specifications.*

Parameter	Measured	Simulated
Rise Time	108 ps	112 ps
BW	4.2 GHz	3.8 GHz
Input C	655 fF	660 fF

Table 2. *Comparison of simulated and measured responses: P7240 with very short ground.*

circuit and is optimized in the P7240 probe design to control the resonant response of the probe for the minimum ground lead inductance case. The model capacitance C1 represents the input capacitance of the custom ASIC that is mounted on the P7240 hybrid circuit. The probe response of the Spice model is picked up off the C1 capacitance, as represented by the "output" label. In the real P7240 probe, the custom ASIC is a buffer amplifier with approximately unity gain that provides both a high input impedance to the measured probe signal and a precision 50 ohm driver for the 50 ohm coax in the 1.4 meter long probe cable. The presence of the custom ASIC buffer coaxial cable driver in the P7240 probe hybrid circuit means that there is no need to include the effect of the probe cable in the P7240 Spice model. Resistor R2 is a simplified representation of the DC resistance of the P7240 probe's input attenuator. The addition of capacitor C2 is used to represent the fact that the P7240 probe ground socket is a floating reference. It is used to represent the physical reality that the probe ground socket is isolated from the probed signal ground by inductor L2 and is also isolated from the oscilloscope measurement ground by the probe cable coax and external shield, which is modeled simply by the addition of capacitance C2.

A comparison between the P7240 Spice model simulation and measured results for the case of a P7240 with no adapters will now be presented. This comparison includes results made using the custom test fixture for both probe loading and probe signal response. Figure 12 shows simulated and measured TDR response waveforms. Note that the simulated and measured TDR plots have been offset slightly in time for ease in distinguishing differences between the simulated and measured response. In this figure, the relatively flat region at the 0 mrho level following the TDR pulse rising edge represents the 50 ohm transmission line in the probe test fixture. The effect of probe loading is shown by the dip in the TDR response in the middle of the 50 ohm transmission line region. Since the TDR response also shows the physical location of the probe loading by time delay from the TDR pulse edge, it can be seen that the probe tip was placed near the center of the transmission

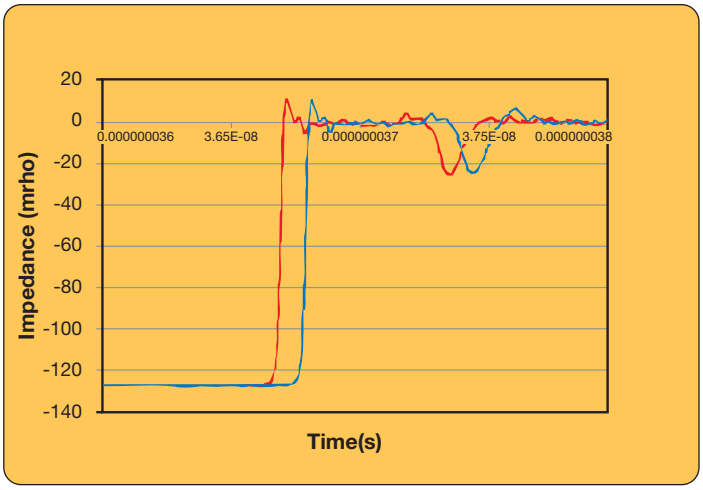
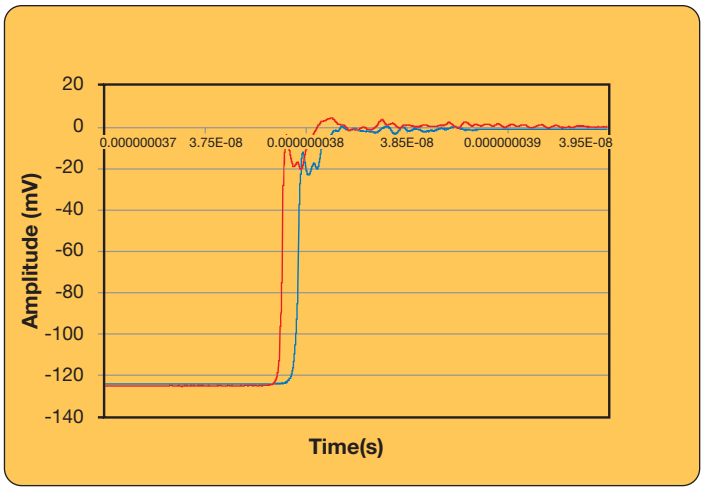
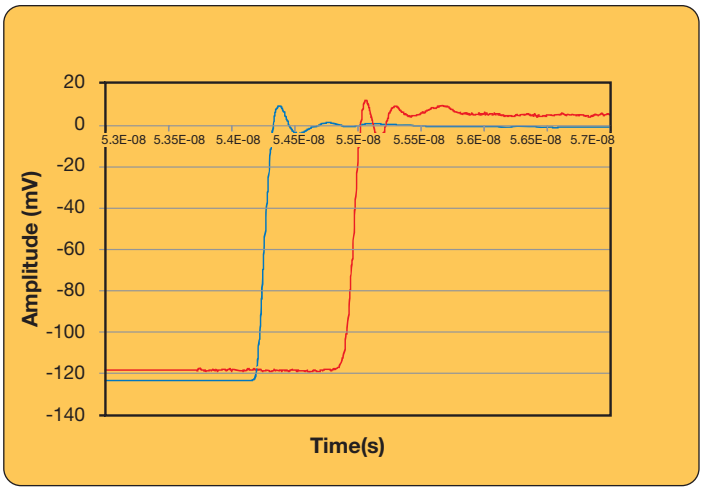


Figure 12. *TDR response: P7240 with very short ground; BLUE: simulation result; RED: measured on scope.*

line span between the input and output connectors of the test fixture. The TDR response dips represent the capacitive loading of the P7240 probe, which shows a good match between the simulated and measured response. By integrating the area of the dip in the probe load response, it is possible to calculate the effective input capacitance of the probe (see Jong, Janko, Tripathi article in the References list, page 27). Figure 13 shows simulated and measured TDT response waveforms. The effect of probe loading is shown by the aberration in the normally flat TDR pulse response. This aberration immediately following the rising edge of the TDR pulse results from probe loading effects on the TDR pulse signal as it propagates down the custom test fixture transmission line. Again there is a good match between the simulated and measured response. Figure 14 shows simulated and measured probe signal response waveforms. The P7240 probe simulated and measured response should match pulse rise time, pulse aberrations, and bandwidth measured with a network analyzer rather than the TDR pulser. Table 2 shows the comparison between simulated and measured data for this minimum inductance model.



▶ ***Figure 13.*** *TDT Response: P7240 with very short ground; BLUE: simulation result; RED: measured on scope.*



▶ ***Figure 14.*** *Probe response: P7240 with very short ground; BLUE: simulation result; RED: measured on scope.*

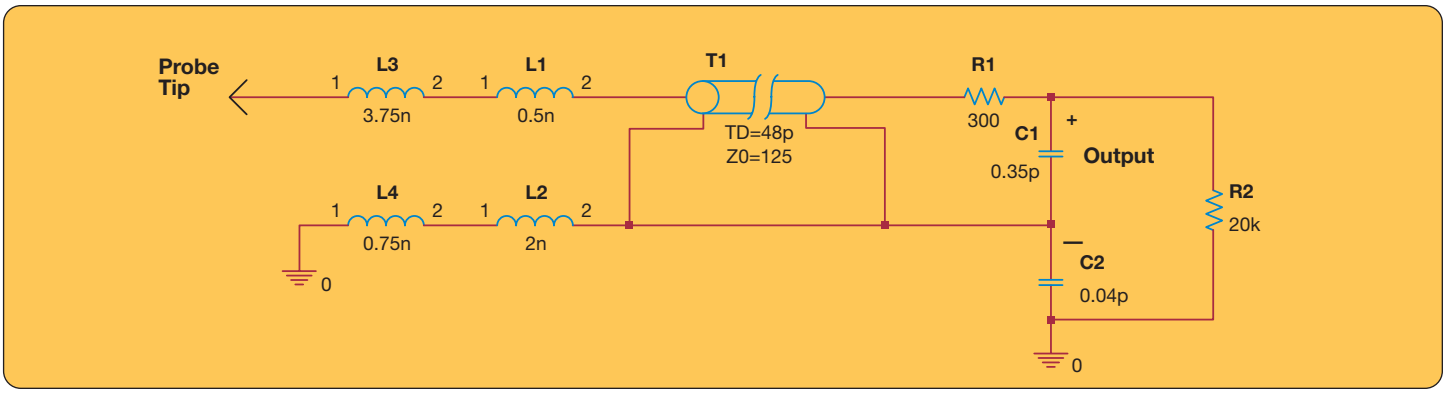


Figure 15. *P7240 with probe tip and pogo ground.*

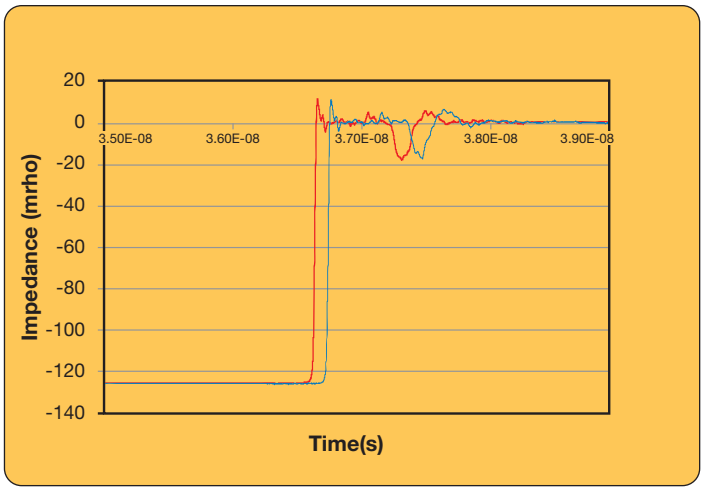
Parameter	Measured	Simulated
Rise Time	122 ps	125 ps
BW	3 GHz	2.95 GHz
Input C	690 fF	700 fF

Table 3. *Comparison of simulated and measured response: P7240 with probe tip and pogo ground.*

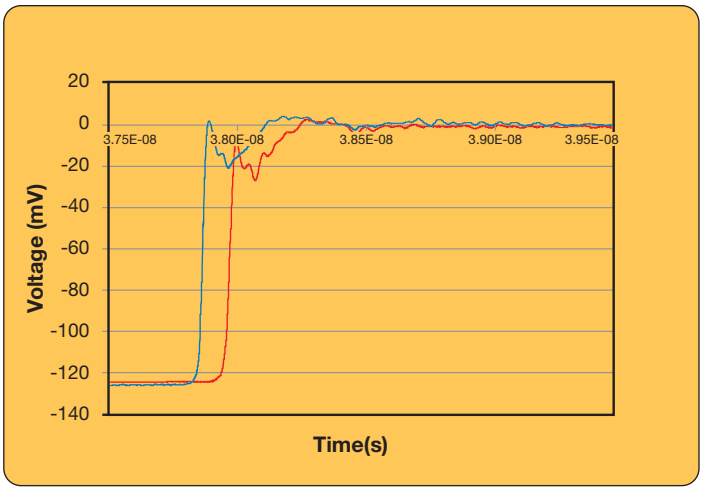
Figure 15 shows the Spice model for the case of a P7240 with probe tip and pogo ground pin. Comparing this model with the minimum inductance model in Figure 11, it can be seen that several of the model element values have changed. One obvious change is additional inductance in both the probe tip and probe ground paths, as might be expected from the additional probe tip and probe ground lead length. The change in damping resistance and changes to the model's transmission line parameters are not as easily explained. Since the Spice model for the probe was developed to fit measurement results to simulated results rather than being fully extracted from the physical structure of the probe, it should not be a complete surprise that changes to the model may not exactly track physical changes to the probe tip/ground adapter configuration. A comparison between the P7240 Spice model simulation and measured results for the case of a P7240 with probe tip and pogo ground pin will now be presented. This comparison again includes results made using the custom test fixture for both probe loading and probe signal response. Figure 16 shows simulated and measured TDR response waveforms. The TDR response dips represent the capacitive loading of the P7240 probe, which shows a good match between the simulated and measured response. Although it may not be obvious simply from inspection, there was only a small increase in calculated input capacitance related to the area of the capacitive dip in the TDR response.

Figure 17 shows simulated and measured TDT response waveforms. Again there is a good match between the simulated and measured TDT response. As might be expected from the small increase in calculated input capacitance, there is only a relatively slight change in the shape of the TDT response aberration. Figure 18 shows simulated and measured probe signal response waveforms. Here there is a much larger change in the probe signal response when compared to the minimum inductance topology result in Figure 14. Although the input capacitance changed only slightly, the added inductance in the probe tip and ground leads made a significant change in the probe input resonant frequency, and resulted in a much larger overshoot and ringing in the probe's pulse response. Table 3 shows the comparison between simulated and measured data for this probe tip and pogo ground pin model.

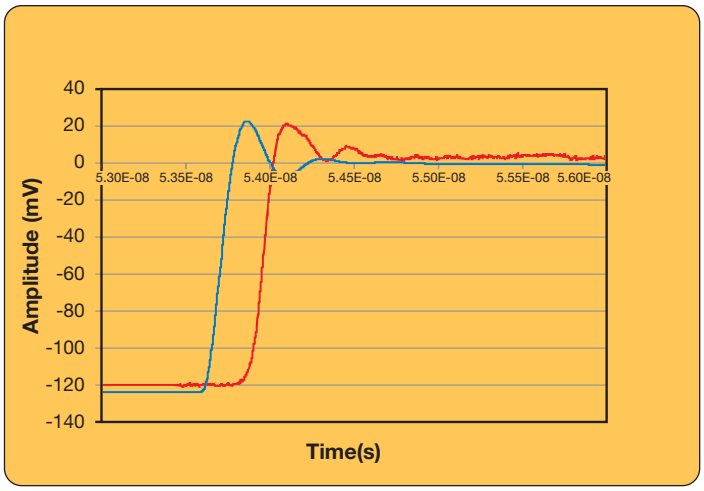
No Spice model will be presented for the case of a P7240 with probe tip and 3-inch ground lead since the probe exhibits such a large resonant response for the very fast pulse rise time used in the probe model development. High speed measurements with a 3-inch ground lead are also significantly affected by the positioning of the ground lead, with enough variation to make the results very difficult to duplicate. However, some probe response measurements will be showing both the poor response with a very fast rise time pulse, as well as the somewhat improved



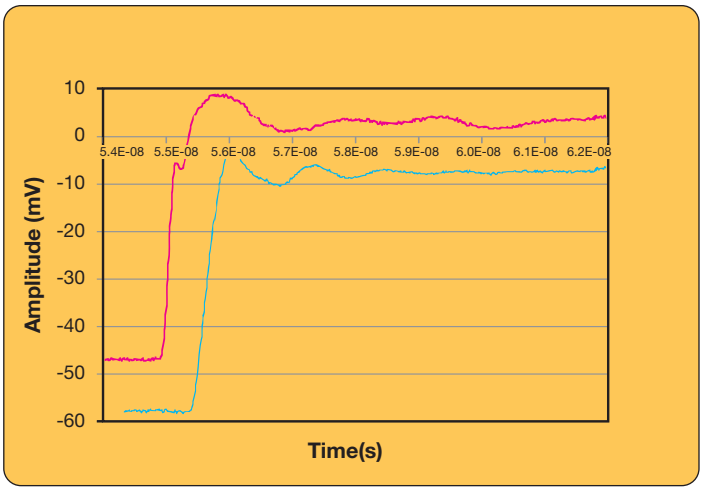
▶ ***Figure 16.*** *TDR response: P7240 with probe tip and pogo ground pin; BLUE: simulation; RED: measured on scope.*



▶ ***Figure 17.*** *TDR response: P7240 with probe tip and pogo ground; BLUE: simulation; RED: measured on scope.*



▶ ***Figure 18.*** *Probe response: P7240 with probe tip and pogo ground; BLUE: simulation; RED: measured on scope.*



▶ ***Figure 19.*** *P7240 with probe tip and 3-inch ground measuring a 25 ps input signal (MAGENTA) and a 750 ps input signal (BLUE).*

response with a slower rise time stimulus. Unlike the poor probe pulse response, the probe loading effects for the 3-inch ground lead case are still not unreasonable. Although not shown in a separate figure, the TDR response for the 3-inch ground lead case is very similar to the pogo ground pin case in that the input capacitance loading is only slightly worse than the minimum inductance case. Figure 19 shows a composite probe response plot for the P7240 with probe tip and 3-inch ground lead for two different pulse input rise times. The two response plots have been shifted in time and offset in amplitude so that the differences can be seen without overlapping.

The 25 ps rise time response plot shows the larger pulse response overshoot and the longer and most visible ringing. It should also be noted that the duration of the pulse response aberrations is related to the relatively long period of the probe input resonance with its long ground lead, rather than the fast response characteristics normally associated with a high performance probe. The 750 ps rise time response plot has a slower probe response rise time but much less overshoot and ringing. As can be seen from these two plots, using a high performance probe like the P7240 with a 3-inch ground lead should be done only with great care. For fast rise time signals, the resonant effects seen when

using a P7240 probe with a 3-inch ground lead will result in significant pulse measurement distortion. For slower rise time signals, the use of a 3-inch ground lead with the P7240 probe may be acceptable, depending on the actual rise time of the input signal and the amount of distortion that can be tolerated. It should also be noted that with a high performance probe like the P7240, the measured signal response can even be affected to some degree by the placement of the user's hand on the probe. For example, holding the probe by the hand nearer to the tip end of the probe head body tends to provide the highest frequency performance. Holding the probe nearer to the cable end of the probe head body tends to change the high frequency environment enough to get a somewhat worse response. This somewhat subtle probe handling effect becomes all the more pronounced when longer probe leads, like the 3-inch ground adapter, are used with the P7240. The exact placement of the ground lead as well as the handling of the probe can affect the measured pulse aberrations. The ultimate guideline for best signal fidelity with a high performance probe like the P7240 is to use as short a ground lead as possible. Another important guideline for signal fidelity is that measurement ground test points should be placed near critical signal test points in all high performance designs.

Summary

This paper has attempted to present the major issues that complicate today's high performance circuit design and measurement. It has reviewed the most common signal integrity noise problems. It has also focused on signal fidelity issues that affect the accurate representation of a signal in a measurement system. Finally, the paper has considered the use of simulation as a means of understanding some of these high performance design issues and providing insight into the effects of circuit board layout on design performance. The need to verify simulation results with physical measurements cannot be stressed enough as well as the need to consider probe loading and probe response limitations in obtaining accurate measurements. To assist the designer in including the effects of probe attachment on design simulation and measurement, probe modeling techniques have been introduced. A specific example of modeling the high performance P7240 TekConnect probe with several different adapter configurations has been presented along with both simulated and measured results.

The probe models in this paper support Tektronix' ongoing commitment to providing the complete solution for our customers. The most up-to-date versions of the P7240 probe models described in this paper can be found on the Tektronix website. It is Tektronix' intention to provide probe models for other high performance probes such as the P7330 3.5 GHz differential probe and the P7260 6 GHz single-ended active probe.

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Contact Tektronix:

ASEAN Countries & Pakistan (65) 6356-3900

Australia & New Zealand (65) 6356-3900

Austria +43 2236 8092 262

Belgium +32 (2) 715 89 70

Brazil & South America 55 (11) 3741-8360

Canada 1 (800) 661-5625

Central Europe & Greece +43 2236 8092 301

Denmark +45 44 850 700

Finland +358 (9) 4783 400

France & North Africa +33 (0) 1 69 86 80 34

Germany +49 (221) 94 77 400

Hong Kong (852) 2585-6688

India (91) 80-2275577

Italy +39 (02) 25086 1

Japan (Sony/Tektronix Corporation) 81 (3) 3448-3111

Mexico, Central America & Caribbean 52 (55) 56666-333

The Netherlands +31 (0) 23 569 5555

Norway +47 22 07 07 00

People's Republic of China 86 (10) 6235 1230

Poland +48 (0) 22 521 53 40

Republic of Korea 82 (2) 528-5299

Russia, CIS & The Baltics +358 (9) 4783 400

South Africa +27 11 254 8360

Spain +34 (91) 372 6055

Sweden +46 8 477 6503/4

Taiwan 886 (2) 2722-9622

United Kingdom & Eire +44 (0) 1344 392400

USA 1 (800) 426-2200

For other areas, contact Tektronix, Inc. at: 1 (503) 627-7111

For further information, contact:

Tektronix, Inc., P.O. Box 500, Beaverton, Oregon 97077-0001, USA, 1 (800) 426-2200.
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